REMARKS

Claims 1-13, 20, and 31-41 are currently pending in the application. Claims 8-12 and 32-41 were withdrawn from consideration by the Examiner as being directed to a non-elected invention or species. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

Allowable Subject Matter

Applicants appreciate the indication that claims 2-7 contain allowable subject matter. However, claims 2-7 are not being presented in independent form at this time, because Applicants submit that all of the pending claims are in condition for allowance for the following reasons.

35 U.S.C. §102 Rejection

Claims 1, 13, 20, and 31 are rejected under 35 U.S.C. §102(e) for being anticipated by U.S. Patent Application Publication No. 2003/0219937 issued to Peterson et al. ("Peterson"). This rejection is respectfully traversed.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See MPEP §2131. Applicants submit that Peterson does not show each and every feature of the claims, and does not anticipate the claimed invention.

The present invention relates to a method of (and a substrate for) manufacturing strained and non-strained silicon regions on the same chip. It is known to impart tensile or compressive stress to semiconductor devices to improve device performance. Such stresses may be imparted by forming the devices in areas of strained silicon. However, imparting these stresses may lead

to defects in the areas of strained silicon. Defects can be detrimental in that they degrade the performance of defect-sensitive devices (e.g., DRAM devices), and compromise the production yield of defect sensitive devices. Exemplary implementations of the invention avoid such detrimental effects by allowing high-performance logic devices to be made in strained regions of a chip, while high-quality, defect-sensitive devices are made in non-strained regions of the same chip. Independent claim 1 recites:

> 1. A method, comprising:
> forming a pattern of strained material and relaxed material on a substrate;
> forming a strained device in the strained material; and
> forming a non-strained device in the relaxed material.

Also, independent claim 31 recites:

> 31. An electrical device, comprising:
> a pattern of strained material and relaxed material formed on a substrate;
> a first device formed in the first strained material; and
> a second device formed in the relaxed material.

The Examiner asserts that Peterson discloses these features at FIG. 1C and Paragraph [0007] (Final Office Action, page 2). Applicants respectfully disagree, and submit that Peterson does not disclose forming a strained device in the strained material, and forming a non-strained device in the relaxed material, as recited in claim 1; or, a first device formed in the first strained material, and a second device formed in the relaxed material, as recited in claim 31.

(i) Peterson does not disclose forming devices in the described embodiments of the invention.

Peterson discloses a method for co-fabricating strained and relaxed crystalline and poly-crystalline structures. More specifically, in FIG. 1C, Peterson shows a substrate 102 having a

relaxed layer 104 and a strained layer 110 formed thereon. As such, Applicants acknowledge that Peterson discloses forming a pattern of strained material and relaxed material on a substrate, as recited in claim 1, and a pattern of strained material and relaxed material formed on a substrate, as recited in claim 31.

However, Peterson does not disclose forming a strained device in the strained material, and forming a non-strained device in the relaxed material, as recited in claim 1; or a first device formed in the first strained material, and a second device formed in the relaxed material, as recited in claim 31. In fact, Peterson does not disclose any devices whatsoever in FIG. 1C, or in any other described embodiment of the invention. Instead, Peterson only discloses the strained layer 104 and the relaxed layer 110. Put another way, Peterson only discloses forming a substrate with a strained region and a relaxed region. In no embodiment does Peterson disclose forming a device in the strained material and forming a device in the relaxed material.

The Examiner, in the Response to Arguments section of the Final Office Action, asserts that Peterson discloses forming devices in the Abstract and Paragraph [0007] (i.e., the "Background" section of the Peterson document). More specifically, the Examiner states:

> From the disclosure of the prior art problems and the disclosure of the Peterson invention it self evident that Peterson wanted to incorporate strained devices and relaxed devices (NMOS and PMOS) on a common substrate.
> (Final Office Action, page 4).

Applicants respectfully disagree with this assertion, and submit that the Examiner is applying an incorrect standard for an anticipation rejection under 35 U.S.C. §102. That is to say, what an examiner speculates an author of a document might have "*wanted to incorporate*" in his or her invention is not a proper basis for an anticipation rejection under 35 U.S.C. §102. Instead, as MPEP §2131 makes clear:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See MPEP §2131.
>
> ...
>
> The identical invention must be shown in as complete detail as is contained in the ... claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that Peterson simply does not disclose any device formed in relaxed layer 104 or strained layer 110. Nor are such devices inherently present in the Peterson structure. Therefore, the applied reference fails to disclose each and every feature of the claimed invention, and cannot reasonably be said to anticipate independent claims 1 and 31.

(ii) Peterson does not disclose forming respective devices "in" the respective materials.

Moreover, Applicants submit that Paragraph [0007] of Peterson does not disclose respective devices formed in the respective materials. Even assuming *arguendo* that the NMOS and PMOS devices described by Peterson in Paragraph [0007] are attributable to Peterson's FIG. 1C, there is no disclosure that such devices are formed ***in*** the relaxed layer 104 and strained layer 110. In contrast, in exemplary embodiments of the invention, a strained layer and a relaxed layer are formed on a substrate, as depicted in FIG. 4 (reproduced below). Then, a strained device is formed in the strained material and a non-strained device is formed in the relaxed material, as depicted in FIG. 5 (reproduced below).

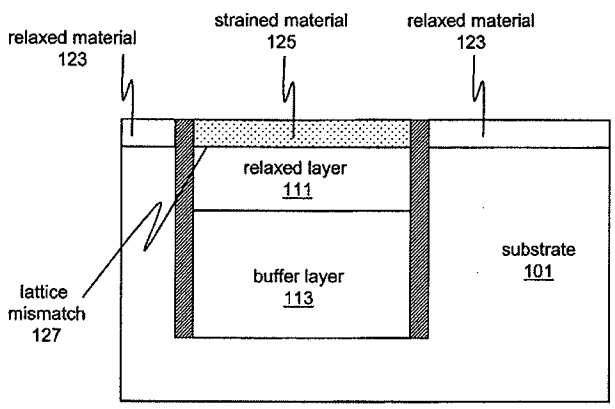


FIG. 4

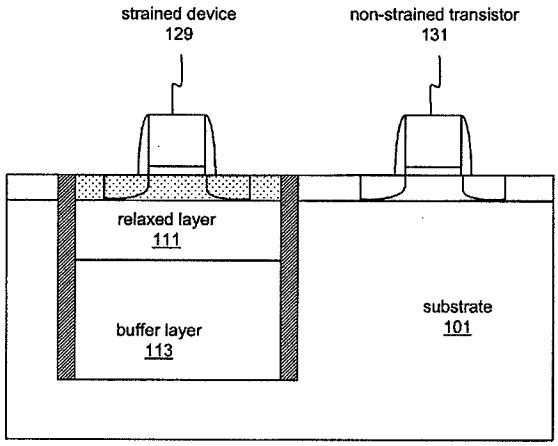


FIG. 5

As is clearly seen in FIGS. 4 and 5, a portion of the strained device is formed in the strained material, and a portion of the non-strained device is formed in the relaxed material. This is not disclosed in Peterson. Applicants acknowledge that Peterson discusses the desirability of having a PMOS device with compressively strained layer. Peterson also separately discusses an NMOS device fabricated over a relaxed layer. However, Petersons's use of the terms "with" and "over" does not constitute a disclosure that these PMOS and NMOS devices are formed in the layers 104, 110 of FIG. 1C. Put another way, Peterson does not disclose anything formed in the relaxed layer 104 or the strained layer 110. Therefore, the applied reference fails to disclose each and every feature of the claimed invention, and cannot arguably anticipate independent claims 1 and 31.

Moreover, the Examiner repeatedly refers to devices formed "on" the strained portion and relaxed portion (see, e.g., page 2, page 3, and page 4 of the Final Office Action). However, the term "on" (used by the Examiner) is not the same as the term "in" (recited in the claimed invention). Therefore, the rejection fails to even address the language of the invention as claimed. However, MPEP §2143.03 states: "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165

USPQ 494, 496 (CCPA 1970). Moreover, 37 C.F.R. 1.104 states: "[t]he examination shall be complete with respect both to compliance of the application or patent under reexamination with the applicable statutes and rules and to the patentability of the invention as claimed ..." (emphasis added). In the case of claims 1 and 31, by asserting that Peterson discloses devices formed "on" instead of "in," the Examiner's rejection fails to address the invention as claimed and is improper in view of 37 C.F.R. 1.104 and MPEP §2143.03.

(iii) Peterson does not disclose a strained device and a non-strained device.

Furthermore, Peterson makes no mention whatsoever of strained and non-strained devices, which are recited in the claimed invention. Again, even assuming *arguendo* that the NMOS and PMOS devices described by Peterson in Paragraph [0007] are attributable to Peterson's FIG. 1C, there is no disclosure that such devices constitute strained and non-strained devices. To the contrary, Peterson merely discloses PMOS and NMOS devices in the Paragraph [0007]; however, there is no disclosure that these PMOS and NMOS devices constitute a strained device and a non-strained device. By comparison, exemplary embodiments of the invention describe a strained device as, for example, a logic device, and a non-strained device as, for example, a memory device (see, for example, Paragraphs [0041] and [0046]), and claims 1 and 31 explicitly recite a strained device and a non-strained device. Peterson, on the other hand, simply does not disclose strained and non-strained devices. Therefore, Peterson fails to disclose all of the features of the claimed invention, and cannot reasonably be said to anticipate independent claims 1 and 31.

For all of the reasons discussed above, Applicants submit that Peterson cannot reasonably be said to disclose forming a strained device in the strained material, and forming a non-strained device in the relaxed material, as recited in claim 1; or, a first device formed in the first strained material, and a second device formed in the relaxed material, as recited in claim 31. Therefore, Peterson does not anticipate the claimed invention.

Applicants submit that claims 13 and 20 depend from allowable claim 1, and are allowable at least for the reasons discussed above with respect to claim 1.

Accordingly, Applicants respectfully request that the §102(e) rejection of claims 1, 13, 20, and 31 be withdrawn.

Request for Rejoinder of Withdrawn Claims

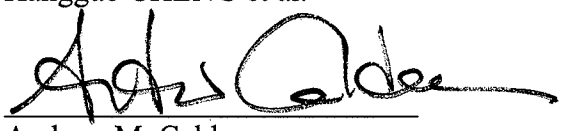
Applicants request that the Examiner rejoin claims 8-12 and 32-41. As discussed above, generic claim 1 is allowable, thus rejoinder of claims 8-12 is proper. Also, because linking claim 31 is allowable for the reasons set forth above, rejoinder of claims 32-41 is proper.

Moreover, as claims 8-12 and 32-41 depend from allowable independent claims, Applicants believe that these claims are patentably distinct from the applied prior art and are in condition for allowance.

CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458

Respectfully submitted,
Kangguo CHENG et al.



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